

Application for United States Letters Patent
for
Temperature Dependent Regulation of Threshold Voltage

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Temperature Dependent Regulation of Threshold Voltage

Field

[0001] The present invention relates to circuits, and more particularly, to analog circuits to provide a transistor body bias voltage.

Background

[0002] Circuits on a die may experience a wide temperature range, where changes in temperature may be both spatial and temporal in nature. This may be of concern in a computer system such as that illustrated in Fig. 1, where die 102 comprises a microprocessor with many sub-blocks, such as arithmetic logic unit (ALU) 104 and on-die cache 106. Die 102 may also communicate to other levels of cache, such as off-die cache 108. Higher memory hierarchy levels, such as system memory 110, are accessed via host bus 112 and chipset 114. In addition, other functional units not on die 102, such as graphics accelerator 116 and network interface controller (NIC) 118, to name just a few, may communicate with die 102 via appropriate busses or ports. Each of these functional units may physically reside on one die or more than one die. Some or parts of more than one functional unit may reside on the same die.

[0003] As operating frequency and transistor integration increase, one or more die used in the computer system of Fig. 1 may experience a wide range of temperatures. This may be of particular concern, but not limited to, microprocessors. The spatial variation in temperature may occur because some circuits (functional blocks) on a microprocessor die may be more active than other circuits (functional blocks) on the same die, thereby consuming more power and leading to so-called "hot spots" on the die. The temporal variation in temperature may occur because some functional units on a die are switched on or off, thereby causing a temporal change in power consumption.

[0004] A temperature change in a transistor, unless compensated for, will change the threshold voltage as well as carrier mobility of the transistor. As temperature decreases, the magnitude of the threshold voltage and carrier mobility increase. This will affect both the OFF (or leakage) current I_{OFF} of the transistor as well as the ON current I_{ON} of the transistor. The effect of temperature change on I_{OFF} is more severe than that of I_{ON} . But the ratio of I_{ON}/I_{OFF} affects performance robustness. Consequently, circuit

designers usually try to keep this ratio greater than some minimum value, e.g., on the order of 100 to 1000, by designing a circuit to operate at its worst-case I_{ON}/I_{OFF} ratio, corresponding to its expected maximum temperature. But when the temperature is lower than its expected maximum, a circuit designed for its worst-case I_{ON}/I_{OFF} ratio will not operate optimally, unless other changes are made to the circuit parameters.

Brief Description of the Drawings

- [0005]** Fig. 1 illustrates a computer system.
- [0006]** Fig. 2 illustrates a cross-sectional view of a body biased pFET.
- [0007]** Fig. 3 illustrates a circuit according to an embodiment of the present invention utilizing biased nFETs.
- [0008]** Fig. 4 illustrates a particular implementation of the embodiment of Fig. 3.
- [0009]** Fig. 5 illustrates a circuit according to an embodiment of the present invention utilizing biased pFETs.
- [0010]** Fig. 6 illustrates a circuit according to another embodiment of the present invention utilizing biased nFETs.
- [0011]** Fig. 7 illustrates a circuit according to another embodiment of the present invention utilizing biased pFETs.

Description of Embodiments

[0012] Because carrier mobility increases with decreasing temperature, a circuit designed for its worst-case I_{ON}/I_{OFF} ratio may be made to operate faster by increasing its clock frequency to take advantage of the increased carrier mobility. However, even greater gains in circuit operation frequency than this may be realized by modulating the threshold voltage as a function of temperature. This can be accomplished by changing the body biasing of transistors as temperature changes. For example, if no changes in body biasing is made, then as temperature decreases, I_{OFF} decreases significantly due to an increase in the magnitude of the threshold voltage. As a result, unless otherwise compensated for, a circuit will operate at a larger I_{ON}/I_{OFF} ratio than necessary. Embodiments of the present invention change the body biasing so as to reduce the magnitude of the threshold voltage when temperature decreases, so that the I_{ON}/I_{OFF} ratio may be brought back (or closer) to the design point (worst-case I_{ON}/I_{OFF} ratio). The frequency of operation of the circuit may then be increased because of the reduction in the magnitude of the threshold voltage. Therefore, by modulating threshold voltage to maintain a fixed I_{ON}/I_{OFF} ratio as temperature changes, the frequency may be maximized for a given temperature.

[0013] Embodiments of the present invention generate a body bias voltage to decrease the magnitude of the threshold voltage when temperature decreases, and to increase the magnitude of the threshold voltage when temperature increases. The body bias may be applied to pFETs, nFETs, or both types of transistors. For example, shown in Fig. 2 is a simplified, cross-sectional view of a pFET using a n-well CMOS process. Substrate 202 is a p-substrate in which n-well 204 (the "body") has been formed. Formed within n-well 204 are source/drain terminals 206. Gate 208 is insulated from n-well 204 by insulator 210. A body terminal (n^+ region 212) is formed within n-well 204 so that the body may be biased at some voltage, denoted as V_{bp} in Fig. 2. Fig. 2 is simplified in that not all layers are shown. (For example, for simplicity, passivation layers are not shown, nor are contacts to source/drain terminals shown.) Any suitable process technology may be utilized to form the transistor of Fig. 2.

[0014] Preferably, V_{bp} should be chosen so as to prevent turning ON the parasitic junction diode formed by the source/drain terminals and the n-well. Typically, the body

bias voltage is in the range $(V_{cc} - 500\text{mV})$ to $(V_{cc} + 500\text{mV})$, where V_{cc} is the supply voltage. The lower end of the range represents forward body biasing so as to decrease the magnitude of the threshold voltage, whereas the upper end of the range represents reverse body biasing so as to increase the magnitude of the threshold voltage.

[0015] In the case of body biasing a nFET, a p^+ region is formed in the channel of a nFET to serve as a body terminal. Again, the body bias voltage should be chosen so as to prevent turning ON the parasitic junction diode formed by the source/drain terminals and the p-substrate. Typically, the body bias voltage is in the range $(V_{ss} - 500\text{mV})$ to $(V_{ss} + 500\text{mV})$, where V_{ss} is the ground of the circuit. The lower end of the range represents reverse body biasing so as to increase the magnitude of the threshold voltage, whereas the upper end of the range represents forward body biasing so as to decrease the magnitude of the threshold voltage.

[0016] An embodiment circuit for body biasing nFETs is shown in Fig. 3, providing at output port 302 the bias voltage V_{bn} to bias the body or bodies of one or more nFETs in another circuit, such as, for example, a functional unit block within a microprocessor. In the circuit of Fig. 3, current mirror 304 provides a gain of A and is biased by nFET 312. The gate of nFET 312 is connected to its drain so that it is biased at I_{ON} . Current mirror 306 provides a gain of B and is biased by nFET 314. The gate of nFET 314 is connected to its source so that it is biased at I_{OFF} . Transistors 312 and 314 are placed relatively close to each other, and to the circuit to be biased, so that they are essentially at the same temperature as the circuit to which V_{bn} is applied.

[0017] In general, transistors 312 and 314 need not have the same width or length. However, it is preferable that they have the same length as each other, and the same length as the transistors to be biased, so that I_{ON} and I_{OFF} track temperature in the same way. If transistors 312 and 314 do not have the same width, then this should be taken into account when setting the current mirror gains so as to realize the desired I_{ON}/I_{OFF} ratio. This will be discussed in more detail later. For the present discussion, assume that transistors 312 and 314 have the same width and length.

[0018] The combination of OPAMP 318 and resistors 320 and 322 provide the input-output functional relationship $V_{bn} = (1 + R_2/R_1)V_1 - (R_2/R_1)V_0$, where R_2 and R_1 are the resistances of resistors 322 and 320, respectively, V_1 is the voltage at node 316

(which is the input port of OPAMP 318), and V_0 is an offset voltage provided at input port 324. The circuit design parameters R_1 , R_2 , and V_0 , as well as A and B , among others, are chosen so that V_{bn} is in the range $(V_{ss} - 500\text{mV})$ to $(V_{ss} + 500\text{mV})$.

[0019] The significance of the current mirror gains is that the path from node 316 through the amplifier comprising OPAMP 318 and resistors 320 and 322, to the body terminals 308 and 310 of nFETs 312 and 314, respectively, and to node 316 via the current mirrors, comprises a negative feedback loop such that under steady state $AI_{ON} = BI_{OFF}$. When steady state is reached, it is also assumed that there is thermal equilibrium, or near thermal equilibrium, locally so that nFETs 312 and 314 are at a well-defined temperature. Thus, A and B are chosen to set the I_{ON}/I_{OFF} ratio, that is, under steady state $I_{ON}/I_{OFF} = B/A$. (This assumes that the various current mirrors are operating in their saturation regions so that current mirrors 304 and 306 are providing constant gains A and B , respectively, and that the other circuit parameters, such as R_1 , R_2 , V_0 , etc., are properly chosen.)

[0020] To describe the negative feedback, suppose the circuit has stabilized at a constant temperature so that $AI_{ON} = BI_{OFF}$. Now suppose there is a sudden decrease in the temperature at nFETs 312 and 314. This will tend to cause a decrease in I_{ON} and a much more significant decrease in I_{OFF} , so that now $AI_{ON} > BI_{OFF}$ and the ratio I_{ON}/I_{OFF} has increased relative to its steady state value. But with current mirror 304 trying to source AI_{ON} into node 316, and with the current mirror comprising nFETs 326 and 328 trying to sink BI_{OFF} from node 316, where $AI_{ON} > BI_{OFF}$, the voltage at node 316 will rise. But a rise in this voltage at node 316 will cause a rise in V_{bn} at output port 302, which is fed back to body terminals 308 and 310. This will increase the forward body bias of nFETs 312 and 314. This increase in forward body bias will decrease the effective threshold voltage of nFETs 312 and 314, which will cause an increase in I_{ON} and a much more significant increase in I_{OFF} so as to decrease the ratio I_{ON}/I_{OFF} .

[0021] Thus, with a sudden temperature decrease that causes an increase in I_{ON}/I_{OFF} , negative feedback will decrease I_{ON}/I_{OFF} . Similar reasoning will show that with a sudden temperature increase that causes a decrease in I_{ON}/I_{OFF} , negative feedback will increase in I_{ON}/I_{OFF} . Consequently, there is negative feedback such that a change in

I_{ON}/I_{OFF} is countered by an opposite change in I_{ON}/I_{OFF} , and the steady state is $AI_{ON} = BI_{OFF}$.

[0022] Current mirrors 304 and 306 may be single-stage current mirrors, but they may also each comprise more than one stage in order to achieve I_{ON}/I_{OFF} ratios of 100 to 1000. An embodiment of these current mirrors is provided in Fig. 4. Here, the combination of transistors 402, 404, 406, 408, 410, and 412 realize current mirror 304; and the combination of transistors 414 and 416 realize current mirror 306. Note that transistors 418 and 420 could be lumped together with transistors 414 and 416 so that the combination of transistors 414, 416, 418, and 420 realize a current mirror. That is, referring to Fig. 3, transistors 326 and 328 and current mirror 306 could be considered together as a current mirror.

[0023] An embodiment providing a bias voltage V_{bp} to bias pFETs is shown in Fig. 5. Current mirror 502 is biased by pFET 504, which has its gate connected to its source to provide a source-drain current I_{OFF} . Current mirror 506 is biased by pFET 508, which has its gate connected to its drain to provide a source-drain current I_{ON} . Note that the current mirrors in Fig. 5 are configured so that a current BI_{OFF} is sourced to node 510 and a current AI_{ON} is sunk from node 510. Node 510 is connected to the non-inverting input port of OPAMP 512, and OPAMP 512 and resistors 514 and 516 are configured to provide the same input-output functional relationship as their counterparts in Fig. 3. However, the values of resistors 514 and 516, as well as the offset voltage V_0 at input port 518 will not, in general, have the same values as their counterparts in Fig. 3. The bias voltage V_{bp} is provided at output port 520, which is fed back to the body terminals 522 and 524 of pFETs 504 and 508, respectively.

[0024] Similar reasoning as considered with respect to Fig. 3 will shown that the path from node 510 through the amplifier comprising OPAMP 512 and resistors 514 and 516, to the body terminals of pFETs 504 and 508, and to node 510 via the current mirrors provides negative feedback so that the circuit of Fig. 5 has a steady state condition such that $AI_{ON} = BI_{OFF}$. Again, as discussed with respect to Fig. 3, the current mirrors in Fig. 5 may comprise single stage or multiple stage current mirrors.

[0025] Various modifications may be made to the disclosed embodiments without departing from the scope of the invention as claimed below. For example, Figs. 6 and 7

provide alternate circuits for providing bias voltages V_{bn} and V_{bp} , respectively. Note that in Figs. 6 and 7, a voltage source follower precedes the OPAMP configuration. In this way, nodes 602 and 702 are not loaded and negative feedback is provided as discussed with respect to the previously disclosed embodiments.

[0026] As another example of a modification to the disclosed embodiments, programmability may be built into the disclosed circuits to allow tuning under various process conditions. For example, current mirrors 304 and 306 in Fig. 3, as well as the other current mirrors in the other disclosed embodiments, may be made programmable by switching various transistors into the current mirrors to vary current mirror gain. This would allow specification of the I_{ON}/I_{OFF} ratio after die fabrication. Also, the OPAMP may also be tuned to apply the correct bias voltage for a given temperature. This could be achieved by varying the offset voltage applied to one of the OPAMP input ports.

[0027] As discussed previously, transistors 312 and 314 need not have the same width. For example, we could let I_{ON} and I_{OFF} represent the ON-current and leakage current per unit transistor width, respectively. Consider Fig. 3 again. Letting W_{ON} denote the width of transistor 312 and W_{OFF} the width of transistor 314, a current $AW_{ON}I_{ON}$ is sourced to node 316 and a current $BW_{OFF}I_{OFF}$ is sunk from node 316. Then, the circuit sets $AW_{ON}I_{ON} = BW_{OFF}I_{OFF}$ so that now $I_{ON}/I_{OFF} = BW_{OFF}/AW_{ON}$. Thus, in the previous circuit descriptions, one may replace A with AW_{ON} and B with BW_{OFF} with the interpretation that I_{ON} is the ON-current per device width and I_{OFF} is the leakage current per device width. The widths and current gains are chosen so that the ratio BW_{OFF}/AW_{ON} provides the desired ratio of ON-current per device width to leakage current per device width.

[0028] It is to be understood in these letters patent that the meaning of " A is connected to B " (A and B as used here are phrases, not the current mirror gains) is that A and B are connected by a passive structure for making a direct electrical connection so that the voltage potentials of A and B are substantially equal to each other. For example, A and B may be connected by way of an interconnect, transmission line, etc. In integrated circuit technology, the "interconnect" may be exceedingly short, comparable to the device dimension itself. For example, the gates of two transistors may be connected to

each other by polysilicon or copper interconnect that is comparable to the gate length of the transistors.

[0029] It is also to be understood that the meaning of “*A* is coupled to *B*” is that either *A* and *B* are connected to each other as described above, or that, although *A* and *B* may not be connected to each other as described above, there is nevertheless a device or circuit that is connected to both *A* and *B*. This device or circuit may include active or passive circuit elements. For example, *A* may be connected to a circuit element which in turn is connected to *B*.

[0030] It is also to be understood that the term “current mirror” may include a single stage current mirror, or a multiple stage current mirror.

[0031] It is also to be understood that various circuit blocks, such as current mirrors, amplifiers, etc., may include switches so as to be switched in or out of a larger circuit, and yet such circuit blocks may still be considered connected to the larger circuit because the various switches may be considered as included in the circuit block.